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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,327	12/29/2000	Paolo Faraboschi	00-BN-054 (STMI01-00054)	7673

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,327	Applicant(s) FARABOSCHI ET AL.	
	Examiner Richard Ellis	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

5. Claims 1-2 and 17-18 are rejected under 35 USC § 102(b) as being clearly anticipated by Crawford et al., U.S. Patent 5,201,043.

Crawford et al. taught (e.g. see figs. 1-5) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

5.1. a data processor (fig. 4) comprising;

5.2. an instruction execution pipeline comprising N processing stages (col. 1 lines 19-22, col. 8 lines 64-67, by stating that the invention is incorporated into an Intel 80486 processor it becomes inherent that there is an execution pipeline because the Intel 80486 processor was pipelined and had N processing stages) capable of executing a load instruction (col. 1 lines 38-47, where a "load instruction" is a kind of "memory reference");

5.3. a status register (fig. 2) capable of storing a modifiable configuration value (fig. 2, 18 AC), said modifiable configuration value having a first value indicating said data processor is capable of executing a misaligned access handling routine and a second

value indicating said data processor is not capable of executing a misaligned access handling routine (col. 6 lines 48-53, col. 7 lines 45-61, fig. 5, 54, 55, 57, and col. 8 lines 51-53);

5.4. a misalignment detection circuit (fig. 5) capable of determining if said load instruction performs a misaligned access to a target address of said load instruction and (col. 8 lines 25-63), in response to a determination that said load instruction does perform a misaligned access, generating a misalignment flag (output of gate 47); and,

5.5. exception control circuitry capable of detecting said misalignment flag and in response thereto determining if said modifiable configuration value is equal to said first value (fig. 5, gate 57 and 63).

6. As to claim 2, Crawford et al. taught that the exception control circuitry, in response to a determination that said modifiable configuration value is equal to said first value, causes said data processor to execution said misaligned access handling routine (col. 8 line 64 to col. 9 line 14).

7. As to claims 17-18, they do not teach or define above the invention claimed in claims 1-2 and are therefore rejected under Crawford et al. for the same reasons set fourth in the rejection of claims 1-2, supra.

8. Claims 9-10 are rejected under 35 USC § 103 as being unpatentable over Crawford et al., U.S. Patent 5,201,043.

9. As to claims 9-10, Crawford et al. taught all the features of the claims that are in common with claims 1-2 and 17-18, as detailed in the rejections above. Additionally Crawford et al. details presence of a memory at col. 1 lines 48-63. Crawford et al. did not specifically detail memory mapped peripherals however it is notoriously well known in the art to provide a computer system with peripherals, and further to memory map those peripherals when it is advantageous to do so, and official notice of such is hereby taken. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have provided

memory mapped peripherals with Crawford et al.'s system because of the well known advantage of memory mapped peripherals of faster access to the peripheral when it is memory mapped.

10. Claims 3-8, 11-16, and 19-20 are rejected under 35 USC § 103 as being unpatentable over Crawford et al., U.S. patent 5,201,043, as applied to claims 1-2 and 17-18, supra., in view of Ross et al., U.S. Patent 5,915,117.

11. As to claim 3, 11, and 19, Crawford et al. did not teach additionally determining if the load instruction was speculative. However, Ross et al. taught determination of a load being speculative (fig. 1, 104).

12. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Ross et al.'s speculative load handling system with Crawford et al.'s system because of Ross et al.'s teachings that performing speculative loads provides for increased processor performance (col. 1 lines 46-58) and additionally taught that speculative loads require special handling of exceptions (col. 1 lines 58-66). Additionally, Ross et al. indicates that load instructions are one of the most important instructions to speculate (col. 3 lines 30-42).

13. As to claims 4, 12, and 20 Crawford et al. in view of Ross et al. taught that the exception control circuitry, in response to a determination that the load instruction was speculative, caused the processor to dismiss the load instruction (Ross et al., fig. 1, 104, 105, 106, 107, 109).

14. As to claims 5 and 13, Crawford et al. in view of Ross et al. taught a data protection unit capable of determining if said load instruction accessed a restricted area of memory (Crawford et al., col. 3 lines 3-6 and col. 3 line 63 to col. 4 line 29).

15. As to claims 6 and 14, Crawford et al. in view of Ross et al. taught that said data protection unit, in response to a determination that said load instruction does access a restricted area of memory, causes said data processor to execute an exception handling routine (Crawford et al. col. 4 lines 19-25).

16. As to claims 7 and 15, Crawford et al. in view of Ross et al. taught that said data protection unit, in response to a determination that said load instruction did access a restricted area of memory (Ross et al. fig. 1, 103) is further capable of determining if said load instruction was speculative (Ross et al. fig. 1, 104).

17. As to claims 8 and 16, Crawford et al. in view of Ross et al. taught that said exception control circuitry, in response to a determination that said load instruction was speculative, caused said data processor to dismiss said load instruction (Ross et al. fig. 1, 105, 106, 107, 109).

18. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

19. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
February 19, 2004